Claims

What is claimed is:

1. An analog-to-digital converter comprising:

at least two quantization stages, wherein a final quantization stage comprises a sigma-delta modulator.

2. The analog-to-digital converter of claim 1, wherein the at least two quantization stages are arranged in a cascade structure.

3. The analog-to-digital converter of claim 2, wherein an input terminal of the sigma-delta modulator is connected to an output terminal of the quantization stage preceding the sigma-delta modulator, and wherein a signal outputted at the output terminal is a function of a quantization noise of the quantization stage preceding the sigma-delta modulator.

4. The analog-to-digital converter of claim 1, wherein an input terminal of the sigma-delta modulator is connected to an output terminal of the quantization stage preceding the sigma-delta modulator, and wherein a signal outputted at the output terminal is a function of a quantization noise of the quantization stage preceding the sigma-delta modulator.

5. The analog-to-digital converter of claim 1, wherein the sigma-delta modulator is a 1^{st} order sigma-delta modulator.

6. The analog-to-digital converter of claim 1, wherein the sigma-delta modulator carries out a 1-bit quantization of its input signal, and carries out highpass-shaping of a quantization error of the sigma-delta modulator.

7. The analog-to-digital converter of claim 1, wherein the sigma-delta modulator carries out highpass-shaping a quantization error of the sigma-delta modulator.

8. The analog-to-digital converter of claim 1, wherein a least significant bit outputted by the sigma-delta modulator contains a delayed input signal $2Q_{N-1}$ and a quantization noise Q_N of the sigma-delta modulator shaped by a term $1-z^{-1}$, and wherein Q_{N-1} is a quantization noise of the quantization stage preceding the sigma-delta modulator.

9. The analog-to-digital converter of claim 1, wherein the sigma-delta modulator shifts its input signal from a first range to a second range.

10. The analog-to-digital converter of claim 1, wherein the sigma-delta modulator is a 2^{nd} order sigma-delta modulator.

11. An analog-to-digital converter comprising:

a plurality of cascaded quantization stages 1 to N, N being a positive integer greater than 1, each quantization stage receiving an input and providing a single output bit representative of its input, a first stage receiving a converter input and providing a most-significant-bit output bit, and the remaining stages receiving an amplified quantization noise signal from a preceding stage; and

a digital block coupled with the quantization stages and receiving the output bits from the quantization stages;

wherein a last quantization stage N comprises a sigma-delta modulator that provides a least-significant-bit output bit and carries out highpass-shaping of a quantization error of the sigma-delta modulator.

12. The analog-to-digital converter of claim 11, wherein the sigma-delta modulator is a first order sigma-delta modulator.

13. The analog-to-digital converter of claim 11, wherein the sigma-delta modulator is a second order sigma-delta modulator.

14. The analog-to-digital converter of claim 11, wherein the least significant bit outputted by the sigma-delta modulator contains a delayed input signal $2Q_{N-1}$ and a quantization noise Q_N of the sigma-delta modulator shaped by a term $1-z^{-1}$, and wherein Q_{N-1} is a quantization noise of the quantization stage preceding the sigma-delta modulator.

15. The analog-to-digital converter of claim 11, wherein the sigma-delta modulator shifts its input signal from a first range to a second range.

16. The analog-to-digital converter of claim 11, wherein an input terminal of the sigma-delta modulator is connected to an output terminal of a quantization stage preceding the sigma-delta modulator, and wherein a signal outputted at the output terminal is a function of a quantization noise of the quantization stage preceding the sigma-delta modulator.

17. An analog-to-digital converter comprising:

a plurality of cascaded quantization stages 1 to N, N being a positive integer greater than 1, each quantization stage receiving an input and providing a single output bit representative of its input, a first stage receiving a converter input and providing a most-significant-bit output bit, and the remaining stages receiving an amplified quantization noise signal from a preceding stage;

wherein a last quantization stage N comprises a sigma-delta modulator that provides a least-significant-bit output bit and carries out highpass-shaping of a quantization error of the sigma-delta modulator.

18. The analog-to-digital converter of claim 17, wherein the sigma-delta modulator is a first order sigma-delta modulator.

19. The analog-to-digital converter of claim 17, wherein the sigma-delta modulator is a second order sigma-delta modulator.

20. The analog-to-digital converter of claim 17, wherein the least significant bit outputted by the sigma-delta modulator contains a delayed input signal $2Q_{N-1}$ and a quantization noise Q_N of the sigma-delta modulator shaped by a term $1-z^{-1}$, and wherein Q_{N-1} is a quantization noise of the quantization stage preceding the sigma-delta modulator.

21. The analog-to-digital converter of claim 17, wherein the sigma-delta modulator shifts its input signal from a first range to a second range.